the input digital reproduction signal, and inputs the reference clock CK to the analog/digital converter 1 and the automatic equalizer 9. The reference clock CK is used as an operation clock in the analog/digital converter 1 and the automatic equalizer 9. On the other hand, the digital reproduction signal input to the transversal filter 4 is transmitted to a decoding circuit after the equalization in the transversal filter 4. In the equalization, the transversal filter 4 is controlled by the tap coefficient as its parameter. The tap coefficient is set from the input digital reproduction signal to the transversal filter 4 and an equalization error which is an error between an output signal from the transversal filter 4 and an equalization target value estimated on the basis of the output signal, in the control unit 5 at appropriate timings. Typically, in the control unit 5 an LMS algorithm for consecutively performing operations on the basis of a steepest descent method so that the square mean of equalization error becomes the minimum, is used.

Please replace the paragraph beginning at page 16, line 13, to page 18, line 8, with the following rewritten paragraph:

The digital information which is recorded on a recording medium is read by a scan of a head not shown, and the read signal is subjected to a processing for emphasizing a predetermined frequency band to result in an analog reproduction signal, which is input to the analog/digital converter 1 to be converted to a multi-value digital reproduction signal. Then, the digital reproduction signal is input to both of the digital phase locked loop 2 and the transversal filter 4 of the automatic equalizer 8. The digital phase locked loop 2 extracts the reference clock CK by the input digital reproduction signal, and inputs the reference clock CK to the frequency divider 3. The frequency divider 3 performs frequency dividing process for performing integral multiplication of the period of the reference clock CK, and outputs a frequency-divided clock CK/N. The frequency-divided clock CK/N is used as the operation clock in the analog/digital converter 1 and the automatic equalizer 8. Here, N denotes the division ratio, and the frequency-division ratio is referred to as N=2 in this first embodiment (hereinafter, referred to as "2-frequency-division"). On the other hand, the digital reproduction signal input to the transversal

filter 4 is transmitted to a decoding circuit after the equalization in the transversal filter 4. In the equalization, the transversal filter 4 is controlled by the tap coefficient as the parameter. The tap coefficient is set from the digital reproduction signal input through the transversal filter 4, and an equalization error which is an error between an output signal from the transversal filter 4 and an equalization target value, in the control unit 5 at approximate timings. Typically, in the control unit 5, an LMS algorithm for consecutively performing operations on the basis of a steepest descent method so that the square mean of equalization error becomes the minimum, is used. As for the equalized waveform output from the transversal filter 4, by using the frequency-divided clock CK/N as the operation clock, the sampling number gets less than that in the case of using the reference clock CK. Thereby, in order to prevent the setting of the equalization target value in the control unit 5 from becoming unstable, the output equalized waveform of the transversal filter 4 is input to the control unit 5, and as well as the straight-line interpolation unit 6 performs interpolation in the output equalized waveform, the signal obtained by interpolating the samples which are omitted due to using the frequency-divided clock CK/N is also input to the control unit 5. Thereby, the setting of the equalization target value can be performed with stability, similarly as in the case of using the reference clock CK.